Remarks

Examiner Berezny is thanked for the thorough Office Action.

IN THE CLAIMS

Parent claims 1, 8 and 16 are amended to added in the last step to add "to form a 1T Static Random Access Memory.". For support see the preamble.

Claim 15 is canceled and rewritten as new claim 16. See below for comments.

Claims 8 and 16 step c 1 is amended to add "said capacitor dielectric comprised of said dielectric layer;" This is to clarify that the dielectric layer is the capacitor dielectric layer in the capacitor plate structure. For support see fig 1, See spec. p. 8 , lines 6 to 19.

Entry is requested to put claim in better condition for allowance for a possible appeal.

CLAIM REJECTIONS:

Rejection of claim 15 under 35 U.S.C. §112

The rejection of claim 15 is acknowledged.

Claim 15 is canceled and rewritten as new claim 16. In claim 16, former claim 15's redundant step d is deleted. Also, Claim 16, step d, is amended to read " said cell node region and said first bit line region do not intersect;" For support see Claim 8 , step b. No new matter is added. Both amendments are correct typographical errors and do not raise new issues.

Entry is requested.

The Rejection Of Claims 1 and 15 Under 35 U.S.C. § 103(a) In View Of Gilgen et al.

The rejection of claim 1 and 15 under 35 U.S.C. § 103(a) in view of Gilgen et al. is acknowledged. Claim 15 is canceled and rewritten as claim 16.

Claims 1 and 16 are non-obvious over Gilgen et al.

Claim 1 and 16 are non-obvious over Gilgen et al. because Gilgen et al. uses non-obvious different steps to form a different structure than claim 1. The table below shows some of the differences between the process of claim 1 and Gilgen et al.

Table: Non-obvious Differences between amended claim 1 and Gilgen et al.

Amended Claim 1	Gilgen et al.
1. (Amended) A method of fabrication of a 1T Static Random Access Memory (SRAM), comprising the steps of:	
a) FIG 1 forming a word line structure 18 24 and a capacitor plate structure 20 30 on a substrate 10;	**Different** – See below. capacitor plate structure 151 161 is over a gate 101 and FOX 71, not on the substrate 11. See fig 16
(1) a capacitor plate structure 20 30 comprised of a capacitor dielectric 20 **on** said substrate 10 and a conductive plate layer 30 on said capacitor dielectric 20; said capacitor plate structure 20 30 overlying a plate region of said substrate; said plate region and said conductive plate layer 30 acting as plates of a capacitor;	**Different** – The capacitor dielectric layer 152 is not no the substrate 11 See fig 16. **Different** – Gilgen's Capacitor bottom plate 151 is a poly layer . In contract, claim 1's capacitor bottom plate is a "plate region" of the substrate.
(b) FIG 2 implanting ions of a first conductivity type into said substrate forming a cell node region 40 in said substrate 10 between said word line structure 18 24 and said capacitor plate structure 20 30; and forming a first bit line region 34 in said substrate adjacent to said word line structure 18 24, said cell node region 40 and said first bit line region 34 do not intersect;	
(c) forming spacers 46 50on the sidewalls of said word line structure 18 24 and said capacitor plate structure 20 30;	**Different** – Spacers 171 161 Fig 17 – spacers 171 are not formed on the capacitor plates 151 161. Also 161 is not a spacer but a cap plate.
d) FIG 3 forming a mask pattern 56 over said cell node 40;	
e) implanting ions of a first conductivity type into said substrate to form a second (high concentration) bitline region 60; and not implanting ions into said cell node;	
f) FIG 4 removing the mask pattern 56;	
g) FIG 4 forming a dielectric layer 52 over said substrate; and	
h) FIG 4 forming a bitline contact 68 to said	

second (high concentration) bitline 60 region **to form a 1T Static Random Access Memory**. .	

- Note the element numbers and fig #'s in the table above do not limit the interpretation of the claim or other claims.

As shown above in the figs, Gilgen does not form the applicant's claimed 1T SRAM device.

Claim 1, step a, is non-obvious because Gilgen's capacitor plate structure 151 161 is over a gate 101 and FOX 71, not on the substrate 11. See fig 16. **One skilled in the art would not interpret Claim 1's term "substrate" to include Gilgen's poly bottom plate 151. gate 101 nor FOX 71**

Claim 1, step a) (1) is non-obvious because **Gilgen's** capacitor dielectric layer 152 is not the substrate 11 See fig 16. Also, Gilgen's Capacitor bottom plate 151 is a poly layer . In contrast, claim 1's capacitor bottom plate is a "plate region" of the substrate.

Claim 1, step c is non-obvious because Gilgen's Spacers 171 161 Fig 17 – spacers 171 are not formed on the capacitor plates 151 161. Also 161 is not a spacer but a poly cap plate.

Furthermore, spacers are a term of art. The interpretation in the Office action is contrary to the meaning of spacers known to those skilled in the art.

There are addition non-obvious differences seen in Gilgen's figs. Most importantly, Gilgen does not form applicant's claimed 1T SRAM.

Claim 16 has the same and more limitations as claim 1. Claim 16 is non-obvious for the reasons above given for claim 1.

Rejection of claims 2, 5-7 under 35 U.S.C. § 103(a) as being unpatentable over Gilgen as applied to claim 1 and further in view of Mandelman

The rejection of claims 2, 5-7 under 35 U.S.C. § 103(a) as being unpatentable over Gilgen as applied to claim 1 and further in view of Mandelman is acknowledged. Reconsideration and withdrawal of the rejection is respectfully requested in view of the following comments.

Claims 2 and 5-7 state: (element numbers added)

2 The method of claim 1 wherein said second bit line region 60 preferably has an impurity concentration greater than the cell node region 40 by at least a factor of 10.

5. The method of claim 1 wherein said second bitline region 60 has a concentration between 1E20 and 1E21 atom/cc.

6. The method of claim 1 wherein said first bit line region 34 has a p-type doping and has an impurity concentration between 1E18 and 1E 19 Atoms/cc, said second bit line region 60 has a p-type doping and has a impurity concentration between 1E20 and 1E21 atoms/cc and said cell node region 40 has a p-type doping and has an impurity concentration between 1E18 and 1E19 atom/cc.

7 The method of claim 1 wherein said first bit line region 34 has a p-type doping and has an impurity concentration between 1E18 and 1E 19 Atoms/cc, said second bit line region 60 has a p-type doping and has a impurity concentration between 1E20 and 1E21 atoms/cc and said cell node region 40 has a p-type doping and has an impurity concentration between 1E17 and 1E18 atom/cc.

First, it is not obvious to combine the references. Neither reference suggest they be combined, nor do they solve related problem. Importantly, neither reference forms applicant's 1T-SRAM cell.

Mandelman forms a different device, a n-type MOSFET for a DRAM, Not applicant's 1T-SRAM cell. See Mandelman claim 1 preamble, background of invention.

Mandelman forms N doped regions in contrast to applicant's N-type node and bitline. The Office Action para. 10 posits that it known in the art to switch N and P type devices. However, while n and p devices are know, it is not known to switch p and n dopants because N and P dopants and type device have different electrical properties. This is especially true with doping concentration. Therefore, is it not obvious to switch doping types. This switch could only be done by hindsight.

Moreover, Mandelman does not for the same 1T-SRAM device as the applicant and it is not obvious to apply the teaches of Mandelman to the applicant's invention. For example, Mandelman performs a N+ implant into the bitline to lower the resistance of W

studs. See col. 3, 60-64. There is no motivation to do this implant in the applicant's device. Moreover, Mandelman does not suggest the advantage of an implant in applicants' 1T SRAM cell.

Claims are non-obvious

Unexpected results.

The applicant's claimed concentrations are not obvious because they provide unexpected results.

> Next, we implant ions of a first conductivity type into the substrate to form a high concentration bitline 60. The high concentration bitline 60 preferably has p-type doping (e.g., boron) and preferably has a concentration between 1E20 and 1E21 Atom/cc. This is at the P plus (p+) doping level. It is critical that these ions are not implanted into the cell node 40.
>
> The second bit line region 60 preferably has an impurity concentration greater than the cell node region 40 by at least a factor of 10.
>
> **The inventors have found an unexpected increase in the performance of the SRAM with the low concentration cell node region 40 and the second (higher concentration) bit line 60 . By blocking the P plus (P+) implant into the cell node, the n-p junction (cell node junction) leakage was unexpectedly and dramatically reduced and the cell data retention time increased.**

See spec. p. 10, lines 8 to 23.

Applicant found an unexpected result by using the claimed dopant types and claimed dopant concentrations. See claims 2-7. See spec. p. 10, L 18 -23. Mandelman does not suggest this.

Also see spec. p 12, lines 13-15.

Furthermore, see arguments in response to Office Action dated 12/3/02, page 6.

Rejection of claims 3 and 4 under 35 U.S.C. § 103(a) as being unpatentable over Gilgen, Mandelman and Chi

The rejection of claims 3 and 4 under 35 U.S.C. § 103(a) as being unpatentable over Gilgen, Mandelman and Chi is acknowledged. Reconsideration and withdrawal of the rejection is respectfully requested in view of the amendments.

Claims 3 and 4 state:

3 The method of claim 1 wherein said substrate 10 is doped with a second conductivity type impurity; second conductivity type impurity is an n-type impurity; said substrate has an impurity concentration between 1E17 and 1E18 atoms/cc.

4 The method of claim 1 wherein said substrate 10 is p doped and has a n-well under said word line structure 18 24 and said capacitor plate structure, said N-well is doped with a second conductivity type impurity; second conductivity type impurity is an n-type impurity; said n-well has an impurity concentration between 1E17 and 1E18 atoms/cc.

First, it is not obvious to combine the references. Neither reference suggest they be combined, nor do they solve related problem. Importantly, neither reference forms applicant's 1T-SRAM cell.

Second, it is further non-obvious to apply Chi to the invention and the other references because Chi does not even form the applicant's p-type device. The Office Action para 5 admits that Chi forms the wrong (n-type) devices. For the reasons stated above, it is not obvious to switch n to p, especially in wells concentrations.

For these reasons the claims are non-obvious.

Rejection of claims 8 under 35 U.S.C. § 103(a) as being unpatentable over Gilgen, Mandelman and Chi and further in view of Wolf, vol. 2, p. 589

The rejection of claims 8 under 35 U.S.C. § 103(a) as being unpatentable over Gilgen, Mandelman and Chi and further in view of Wolf, vol. 2, p. 589 is acknowledged. Reconsideration and withdrawal of the rejection is respectfully requested in view of the comments.

The combination of 4 references, none which form applicant's claimed 1T SRAM is further indication of the non-obvious combination of references to meet the claims.

Claim 8 contains the limitationd of non-obvious claims 1 to 7. Claim 8 is non-obvious for the reasons discussed above.

Response to Arguments in Office Action dated 12/3/2002

The Claim's "substrate" is not interpreted to include Gilgen's bottom polysilicon capacitor plate 151

On page 6, paragraph number 8, the Office Action posits that in the applicant's claims' the term " substrate" could be interpreted as including Gilgen's bottom polysilicon capacitor plate 151 (See e.g., Gilgen fig 16). However, applicant argues that this is not a interpretation one skilled in the art would have and is a strain interpretation. See MPEP 2111. In interpreting Gilgen's to meet claim 1 step a, one skilled in the art would read Gilgen's substrate 11 as the substrate. Gilgen is one skilled in the art. Gilgen interprets the substrate 11 to be a separate element from the Gilgen's poly capacitor plate 151 col. 8 L 54. See Giligen's fig 14 – 16.

Furthermore, the claims are interpreted in light of the spec. The specification describes substrate and gives examples. See spec. p. 7, L 12-23. See fig 1. One skilled in the art, would not include Gilgen't poly bottom plate forms over several structures and Gilgen's substrate 11 as part of the substrate of claims 1 , 8 and 15.

Claim 1, step c, is not meet – Gilgin does not form spacers on Capacitor structure sidewalls.

Applicant's Claim 1, step c and corresponding steps in other parent claims 8 and 15, are not meet because Gilgen does not form spacers on Capacitor (cap) structure sidewalls. The Office Action argues that Gilgen capacitor plate 161 serves as a sidewall spacer on Gilgen capacitor structure. However, this is incorrect if Gilgen structure is consistently analyzed.

First, Gilgen's cap structure 161 152 includes capacitor plate 161 and cap dielectric 152. See Gilgen fig 16 and see OA page 2, para 4, lines 4 -6 of para 4. The Office Action then posits that spacers 171 161 are formed on the sidewalls of the capacitor structure 161 152. However, this is not shown nor suggested by Gilgen and contrasts with Claim 1, steps a and c. Gilgen can not and does not first form cap plate161 and then form a second time cap plate 161 (a spacer). See Gilgen figs 15 to 18. See Gilgen col. 8., line 141. Gilgin forms the cap plate 161 only one time. In contrast, the Office Action page 2 and 3 posits that Gilgin forms the cap plate 161 two times, first as a cap plate 161 and then a second time as a spacer 161. Applicant respectfully urges that this is a strained and inconsistent interpretation of Gilgin and applicant's claims.

Second, claim 1, step c and corresponding parent claims state that the "spacers are formed on the sidewalls of the capacitor plate structure." Here, Giligen does not form spacers 161 on the sidewalls of the cap plate structure 152 161, but only on the sidewalls of the cap dielectric layer 152. Therefore claim 1 step c is not meet.

Applicant's amended claims' "1T SRAM" is not suggested by Gilgen.

Amended claim 1 step h and corresponding claims 8 and 16 claim the Applicant's 1T SRAM. This is not suggested by Gilgen.

Furthermore, the amendment does not raise a new issue since, the preamble is read to limit structures and intended uses. See MPEP 211.02 p. 2110-48 to 49.

Applicant agues that it is not obvious to switch dopant types.

The Office action p 7, para 9 , cites Gilgen to show it is obvious to switch dopant types. However, applicant agues that it is not obvious to switch dopant types to applicant's 1T SRAM device. Switching dopant types affects device performances depending on the device made and the operational conditions.

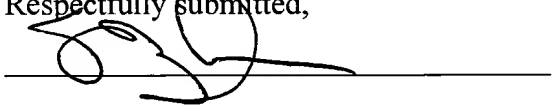
Furthermore, even the dopant concentration for a specified dopant type is important. Applicant found an unexpected result by using the claimed dopant types and claimed dopant concentrations. See claims 2-7. See spec. p. 10, L 18 -23.

CONCLUSION

In conclusion, reconsideration and withdrawal of the rejections are respectfully requested. Allowance of all claims is requested. Issuance of the application is requested.

It is requested that the Examiner telephone the undersigned attorney George Saile at (845) 452-5863 should there be anyway that we could help to place this Application in condition for Allowance.

Respectfully submitted,



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Appendix

Version with markings to show changes

In the Claims

1. (TWICE AMENDED) A method of fabrication of a 1T Static Random Access Memory (SRAM), comprising the steps of:

a) forming a word line structure and a capacitor plate structure on a substrate;

(1) said capacitor plate structure comprised of a capacitor dielectric on said substrate and a conductive plate layer on said capacitor dielectric; said capacitor plate structure overlying a plate region of said substrate; said plate region and said conductive plate layer acting as plates of a capacitor;

b) implanting ions of a first conductivity type into said substrate forming a cell node region in said substrate between said word line structure and said capacitor plate structure; and forming a first bit line region in said substrate adjacent to said word line structure;

c) forming spacers on the sidewalls of said word line structure and said capacitor plate structure;

d) forming a mask pattern over said cell node;

e) implanting ions of a first conductivity type into said substrate to form a second bitline region; and not implanting ions into said cell node;

f) removing the mask pattern;

g) forming a dielectric layer over said substrate; and

h) forming a bitline contact to said second bitline region <u>to form a 1T Static Random Access Memory</u>

8. (TWICE AMENDED) A method of fabrication of a 1T Static Random Access Memory (SRAM), comprising the steps of :

a) forming a dielectric layer on a substrate;

forming a conductive layer on said dielectric layer;

patterning said conductive layer and said dielectric layer to form a word line structure and a capacitor plate structure on a substrate;

(1) said capacitor plate structure comprised of a capacitor dielectric on said substrate and a conductive plate layer on said capacitor dielectric; said capacitor plate structure overlying a plate region of said substrate; said plate region and said conductive plate layer acting as plates of a capacitor; <u>said capacitor dielectric comprised of said dielectric layer;</u>

(2) said substrate is p doped and has a n-well under said word line structure and said capacitor plate structure, said N-well is doped with a second conductivity type impurity; second conductivity type impurity is an n-type impurity; said n-well has an impurity concentration between 1E17 and 1E18 atoms/cc;

b) implanting ions of a first conductivity type into said substrate forming a cell node region in said substrate between said word line structure and said capacitor plate structure; and forming a first bit line region in said substrate adjacent to said word line structure, said cell node regionand said first bit line region do not intersect;

(1) said first bit line region andsaid cell node region have a p-type doping and have an impurity concentration between 1E18 and 1E 19 atoms/cc,

c) forming spacers on the sidewalls of said word line structure and said capacitor plate structure;

d) forming a mask pattern over said cell node;

e) implanting ions of a first conductivity type into said substrate to form a second bitline region; and not implanting ions into said cell node; said second bitline region has a concentration between 1E20 and 1E21 atom/cc;

f) removing the mask pattern;

g) forming a dielectric layer over said substrate; and

h) forming a bitline contact to said second bitline region to form a 1T Static Random Access Memory.

Please cancel claim 15.

Please add claim 16.

16. A method of fabrication of a 1T Static Random Access Memory (SRAM), comprising the steps of:

a) forming a dielectric layer on a substrate;

b) forming a conductive layer on said dielectric layer;

c) patterning said conductive layer and said dielectric layer to form a word line structure and a capacitor plate structure on a substrate;

(1) said capacitor plate structure comprised of a capacitor dielectric on said substrate and a conductive plate layer on said capacitor dielectric; said capacitor plate structure overlying a plate region of said substrate; said plate region and said conductive plate layer acting as plates of a capacitor; said capacitor dielectric is comprised of said dielectric layer;

d) implanting ions of a first conductivity type into said substrate forming a cell node region in said substrate between said word line structure and said capacitor plate structure; and forming a first bit line region in said substrate adjacent to said word line structure, said cell node region and said first bit line region do not intersect;

e) forming spacers on the sidewalls of said word line structure and said capacitor plate structure;

f) forming a mask pattern over said cell node;

g) implanting ions of a first conductivity type into said substrate to form a second bitline region; and not implanting ions into said cell node;

h) removing the mask pattern;

i) forming a dielectric layer over said substrate; and

j) forming a bitline contact to said second bitline region to form a 1T Static Random Access Memory.